

SN74LVC1G32-Q1 单路双输入正或门

1 特性

- 采用具有 0.5mm 间距的小型 1.45mm² 封装 (DRY)
- 支持 5V V_{CC} 运行
- 输入接收高达 5.5V 的电压
- 支持下行转换到 V_{CC}
- 电压为 3.3V 时, t_{pd} 最大值为 3.6ns
- 低功耗, 10μA 最大 I_{CC}
- 电压为 3.3V 时, 输出驱动为 ±24mA
- I_{off} 支持带电插入、局部关断模式和后驱动保护
- 闩锁性能超过 100mA, 符合 JESD 78 II 类规范
- ESD 保护性能超过 JESD 22 规范要求
 - 2000V 人体放电模型 (A114-A)
 - 200V 机器模型 (A115-A)
 - 1000V 充电器件模型 (C101)

2 应用

- AV 接收器
- 蓝光播放器与家庭影院
- 数码相框 (DPF)
- 嵌入式 PC
- IP 电话: 无线
- 高速数据采集和生成
- 电机控制: 高电压
- 光纤网络: 光纤和 EPON 视频
- 个人导航设备 (GPS)
- 便携式媒体播放器
- 专用分支交换机 (PBX)
- 服务器 PSU
- SSD: 内部和外部
- 电视: LCD 电视/数字电视和高清电视 (HDTV)
- 电信方舱: 配电单元 (PDU)、电源监控单元 (PMU)、无线电池监控、远程电动倾斜单元 (RET)、远程射频单元 (RRU)、塔顶放大器 (TMA)
- 视频会议: 基于 IP 的 HD
- 矢量信号分析器和发生器
- WiMAX 和无线基础设施设备
- 无线耳机、键盘、鼠标和中继器

3 说明

按照设计, 此单路双输入正或门可在 1.65V 至 5.5V V_{CC} 下运行。

SN74LVC1G32-Q1 器件以正逻辑执行

$Y = A + B$ or $Y = \overline{A} \cdot \overline{B}$ 布尔函数。

CMOS 器件具有高输出驱动, 同时在宽 V_{CC} 工作范围内保持低静态功率耗散。

SN74LVC1G32-Q1 器件采用多种封装, 包括外形尺寸为 1.45mm × 1.00mm 的小型 DRY 封装。

器件信息

器件名称	封装 (引脚)	封装尺寸
SN74LVC1G32QDBV	SOT-23 (5)	2.90mm × 2.80mm
SN74LVC1G32QDCK	SC70 (5)	2.00mm × 1.25mm
SN74LVC1G32QDRY	SON (6)	1.45mm × 1.00mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



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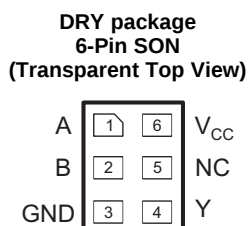
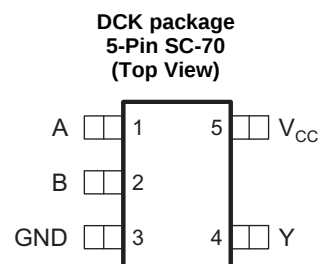
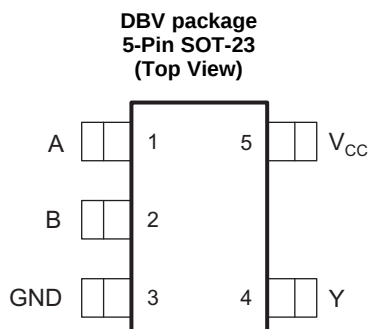
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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (February 2006) to Revision A	Page
• 已更改 根据新的 TI 标准更改了数据表格式	1
• 已添加 在器件信息 表中添加了 SON (6) DRY 封装	1
• Added DRY Package to <i>Pin Configuration and Functions</i> section.	3

5 Pin Configuration and Functions



NC = No Connect

See Mechanical drawings at the end of the data sheet for dimensions

Pin Functions

PIN			DESCRIPTION
NAME	DBV, DCK	DRY	
A	1	1	Input
B	2	2	Input
GND	3	3	Ground
Y	4	4	Output
VCC	5	6	Power pin
NC	–	5	Not connected

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		–0.5	6.5	V
V _I	Input voltage range ⁽²⁾		–0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		–0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾		–0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		–50	mA
I _{OK}	Output clamp current	V _O < 0		–50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

PARAMETER	DEFINITION	VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 3 V to 3.6 V	0.8		
		V _{CC} = 4.5 V to 5.5 V	0.3 × V _{CC}		
V _I	Input voltage	0	5.5		V
V _O	Output voltage	0	V _{CC}		V
I _{OH}	High-level output current	V _{CC} = 1.65 V	–4		mA
		V _{CC} = 2.3 V	–8		
		V _{CC} = 3 V	–16		
			–24		
		V _{CC} = 4.5 V	–32		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		mA
		V _{CC} = 2.3 V	8		
		V _{CC} = 3 V	16		
			24		
		V _{CC} = 4.5 V	32		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20		ns/V
		V _{CC} = 3.3 V ± 0.3 V	10		
		V _{CC} = 5 V ± 0.5 V	5		
T _A	Operating free-air temperature	DSBGA package	–40	85	°C
		All other packages	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC1G32-Q1			UNIT
		DBV	DCK	DRY	
		5 PINS	5 PINS	6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	229	278	439	°C/W
R _{θJCTop}	Junction-to-case (top) thermal resistance	164	93	277	°C/W
R _{θJB}	Junction-to-board thermal resistance	62	65	271	°C/W
ψ _{JT}	Junction-to-top characterization parameter	44	2	84	°C/W
ψ _{JB}	Junction-to-board characterization parameter	62	64	271	°C/W
R _{θJCBot}	Junction-to-case (bottom) thermal resistance	–	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application report](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	–40°C to 85°C			–40°C to 125°C RECOMMENDED			UNIT
				MIN	TYP ⁽¹⁾	MAX	MIN	TYP	MAX	
V _{OH}		I _{OH} = –100 μA	1.65 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1			V
		I _{OH} = –4 mA	1.65 V	1.2			1.2			
		I _{OH} = –8 mA	2.3 V	1.9			1.9			
		I _{OH} = –16 mA	3 V	2.4			2.4			
		I _{OH} = –24 mA		2.3			2.3			
		I _{OH} = –32 mA	4.5 V	3.8			3.8			
V _{OL}		I _{OL} = 100 μA	1.65 V to 5.5 V	0.1			0.1			V
		I _{OL} = 4 mA	1.65 V	0.45			0.45			
		I _{OL} = 8 mA	2.3 V	0.3			0.4			
		I _{OL} = 16 mA	3 V	0.4			0.5			
		I _{OL} = 24 mA		0.55			0.65			
		I _{OL} = 32 mA	4.5 V	0.55			0.65			
I _I	A or B inputs	V _I = 5.5 V or GND	0 to 5.5 V	±5			±5			μA
I _{off}		V _I or V _O = 5.5 V	0	±10			±25			μA
I _{CC}		V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V	10			10			μA
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V	500			500			μA
C _I		V _I = V _{CC} or GND	3.3 V	4			4			pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics, C_L = 15 pF

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	1.9	7.2	0.8	4.4	0.9	3.6	0.8	3.4	ns

6.7 Switching Characteristics, 1.8 V and 2.5V

over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted)⁽¹⁾ (see [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C		–40°C to 125°C RECOMMENDED		–40°C to 85°C		–40°C to 125°C RECOMMENDED		UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.5 V ± 0.2 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	2.8	8	2.8	9	1.2	5.5	1.2	6	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.8 Switching Characteristics, 3.3 V and 5 V

over recommended operating free-air temperature range, $C_L = 30$ pF or 50 pF (unless otherwise noted)⁽¹⁾ (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C		–40°C to 125°C RECOMMENDED		–40°C to 85°C		–40°C to 125°C RECOMMENDED		UNIT
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	1.1	4.5	1	4	1	4	1	4.5	ns

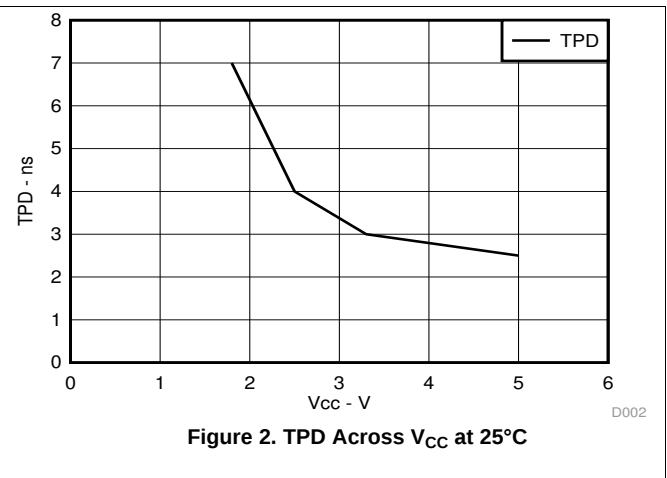
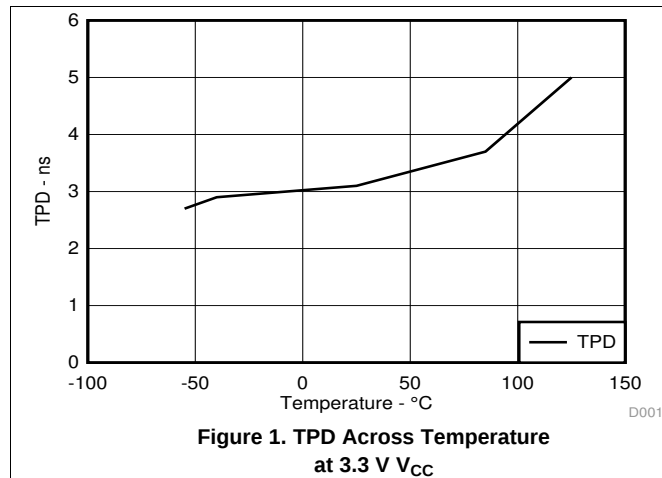
(1) On products compliant to MIL-PRF-38535, this parameter is not production tested

6.9 Operating Characteristics

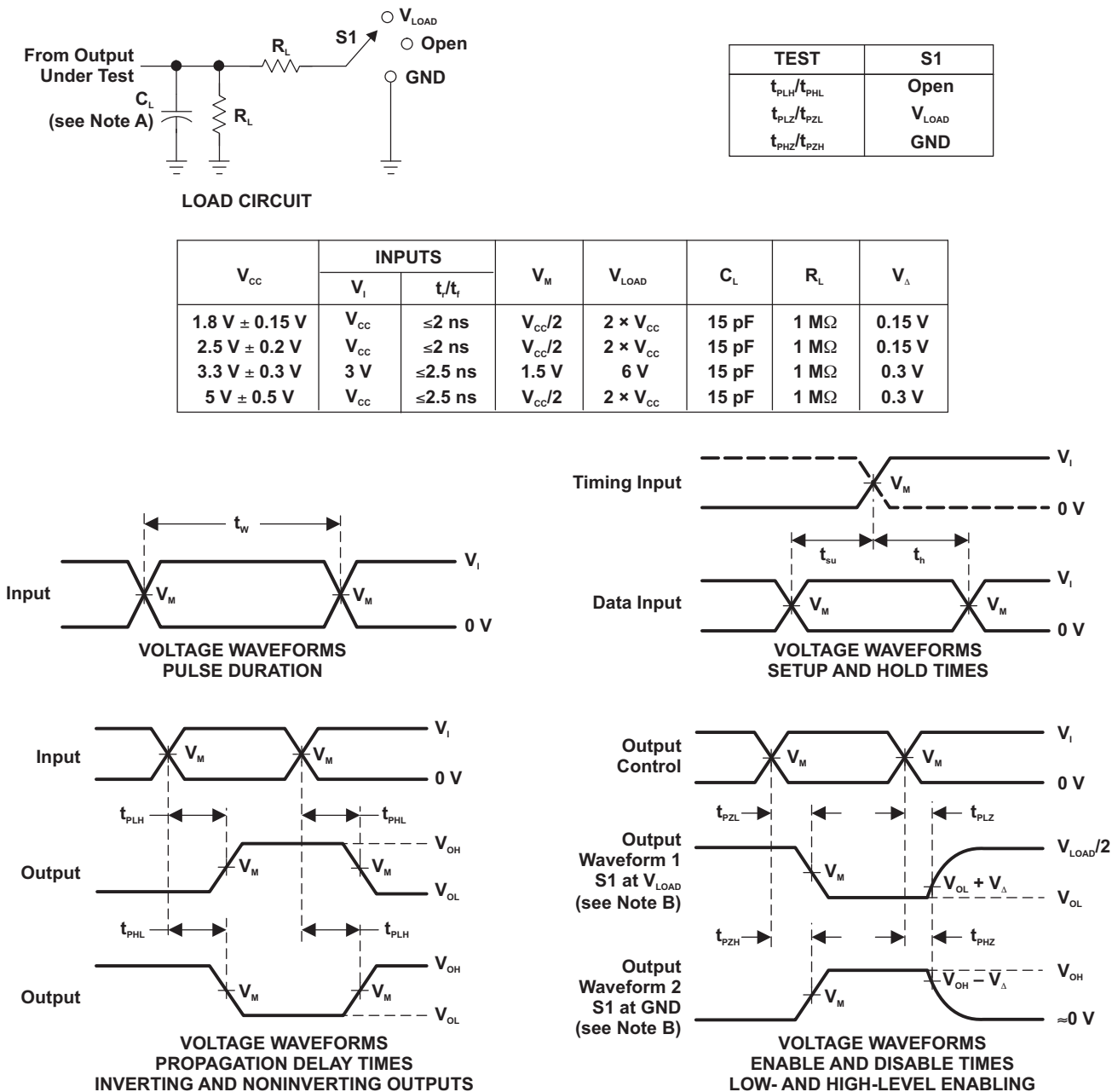
$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8$ V	$V_{CC} = 2.5$ V	$V_{CC} = 3.3$ V	$V_{CC} = 5$ V	UNIT
		TYP	TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	$f = 10$ MHz	20	20	21	22	pF

6.10 Typical Characteristics



7 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

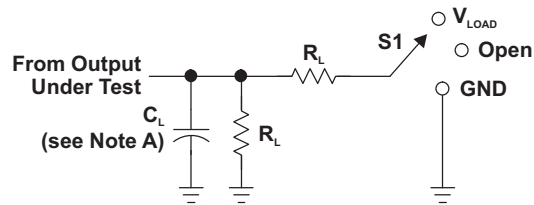
F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. t_{PLH} and t_{PHL} are the same as t_{pd} .

H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

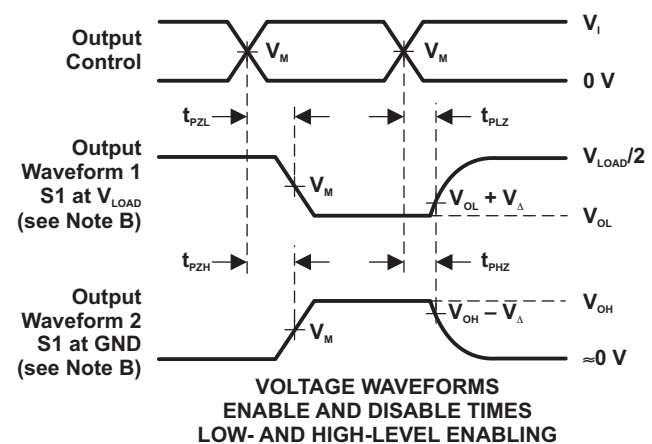
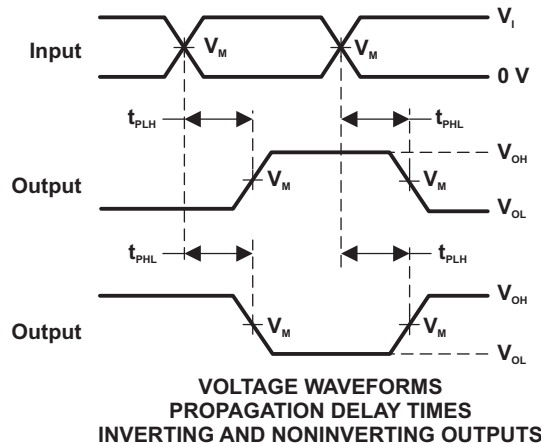
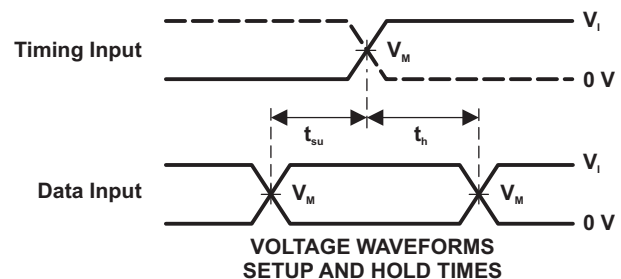
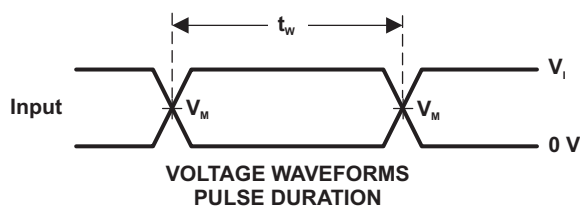
Parameter Measurement Information (continued)



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{on} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC1G32-Q1 device contains one 2-input positive OR gate device and performs the Boolean function $Y = A + B$ or $Y = \overline{A} \cdot \overline{B}$. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram



8.3 Feature Description

- Wide operating voltage range.
 - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

8.4 Device Functional Modes

Table 1. Function Table

INPUTS		OUTPUT Y
A	B	
H	X	H
X	H	H
L	L	L

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G32-Q1 device is a high drive CMOS device that can be used for implementing OR logic with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5-V tolerant allowing translation down to V_{CC} .

9.2 Typical Application

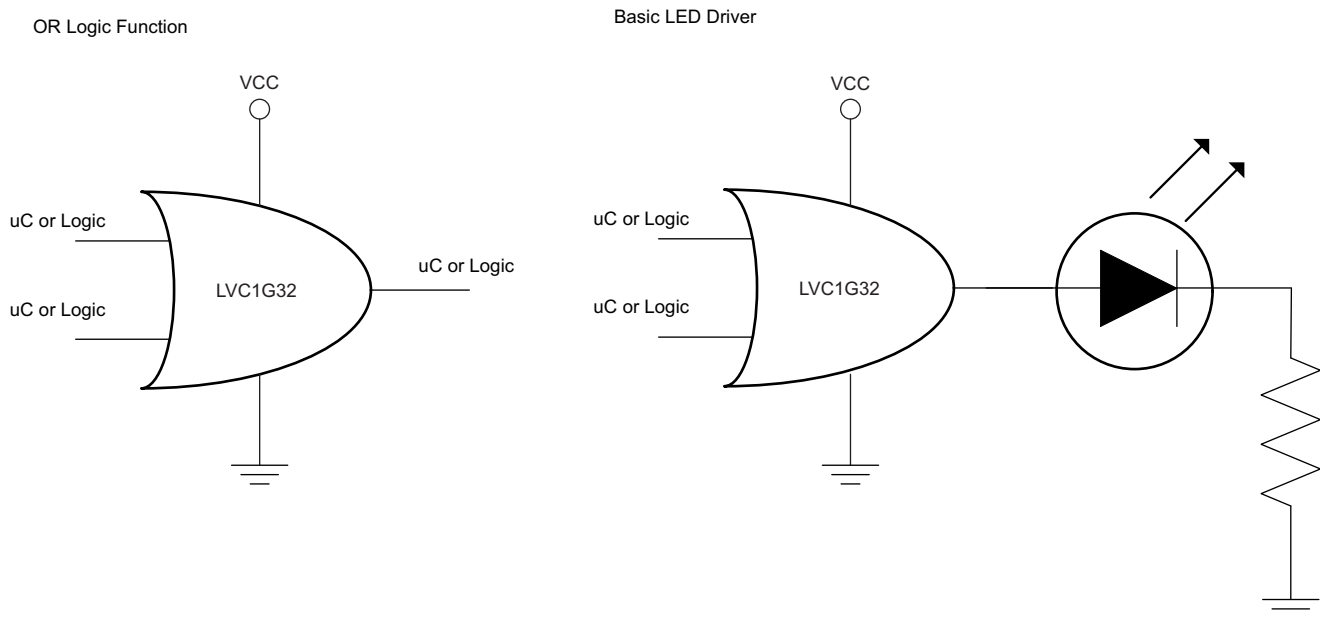


Figure 5. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
 - Rise time and fall time specs. See ($\Delta t/\Delta V$) in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the [Recommended Operating Conditions](#) table at any valid V_{CC} .
2. Recommend Output Conditions:
 - Load currents should not exceed (I_O max) per output and should not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the [Absolute Maximum Ratings](#) table.

Typical Application (continued)

- Outputs should not be pulled above V_{CC} .

9.2.3 Application Curves

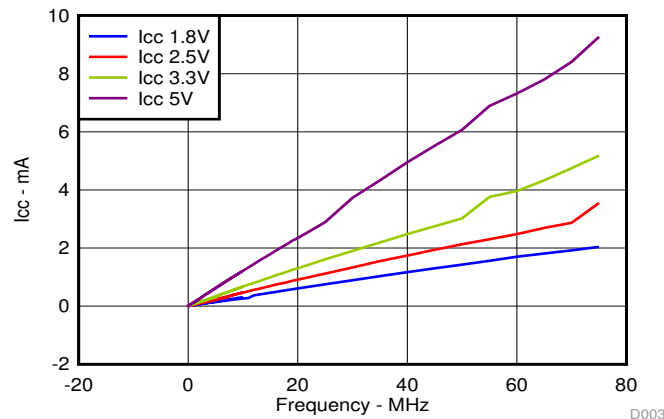


Figure 6. I_{CC} vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F capacitor is recommended. If there are multiple VCC pins, then a 0.01- μ F or 0.022- μ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used, or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Layout Example](#) are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever make more sense or is more convenient.

11.2 Layout Example

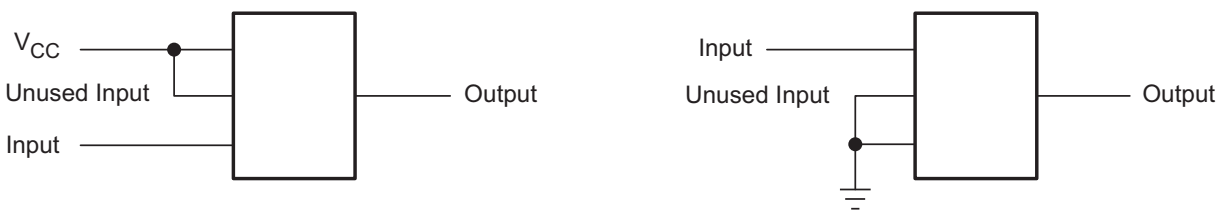


Figure 7. Layout Example

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

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TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G32QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C32O	Samples
SN74LVC1G32QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CGJ, CGO)	Samples
SN74LVC1G32QDRYRQ1	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	FW	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G32-Q1 :

- Catalog : [SN74LVC1G32](#)
- Enhanced Product : [SN74LVC1G32-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G32QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G32QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G32QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G32QDRYRQ1	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G32QDBVRQ1	SOT-23	DBV	5	3000	190.0	190.0	30.0
SN74LVC1G32QDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
SN74LVC1G32QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
SN74LVC1G32QDRYRQ1	SON	DRY	6	5000	189.0	185.0	36.0

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

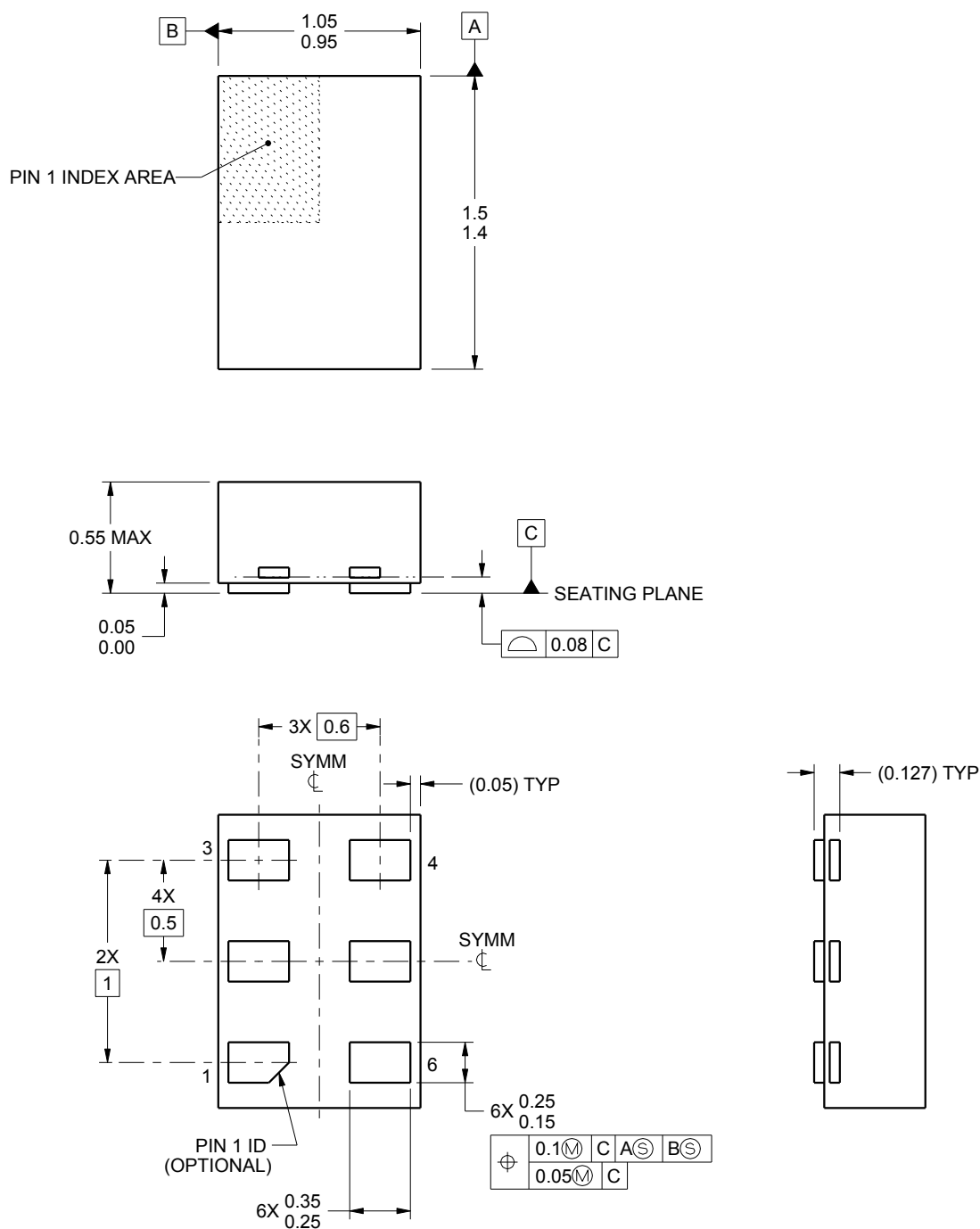
4207181/G



PACKAGE OUTLINE

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222207/B 02/2016

NOTES:

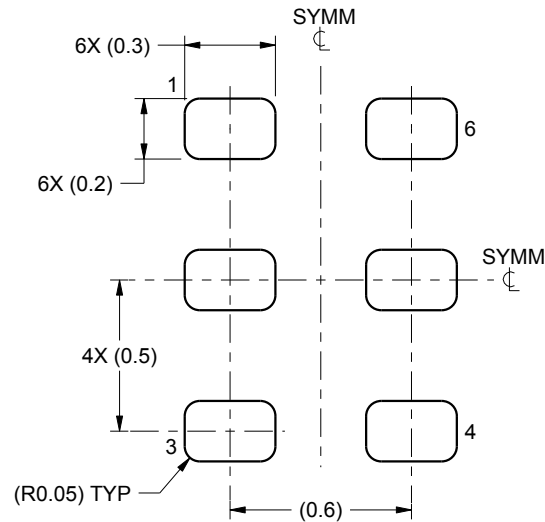
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

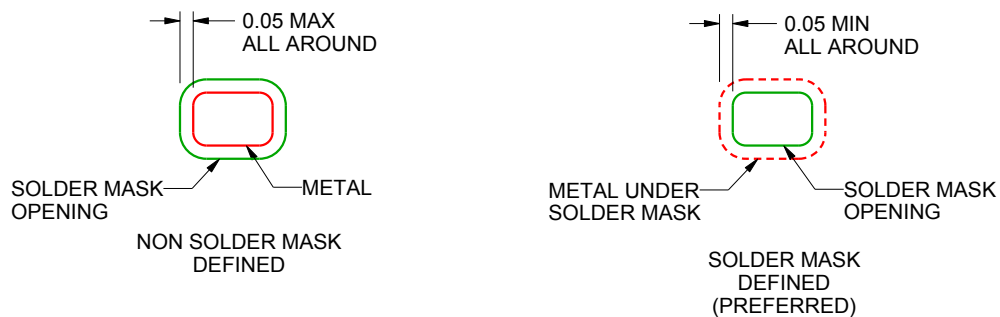
DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X



SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

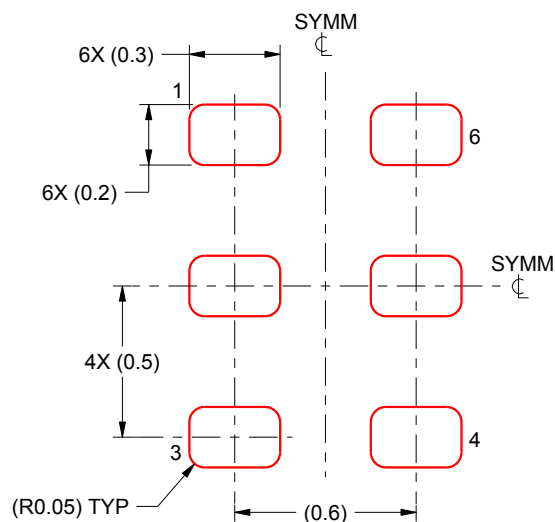
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

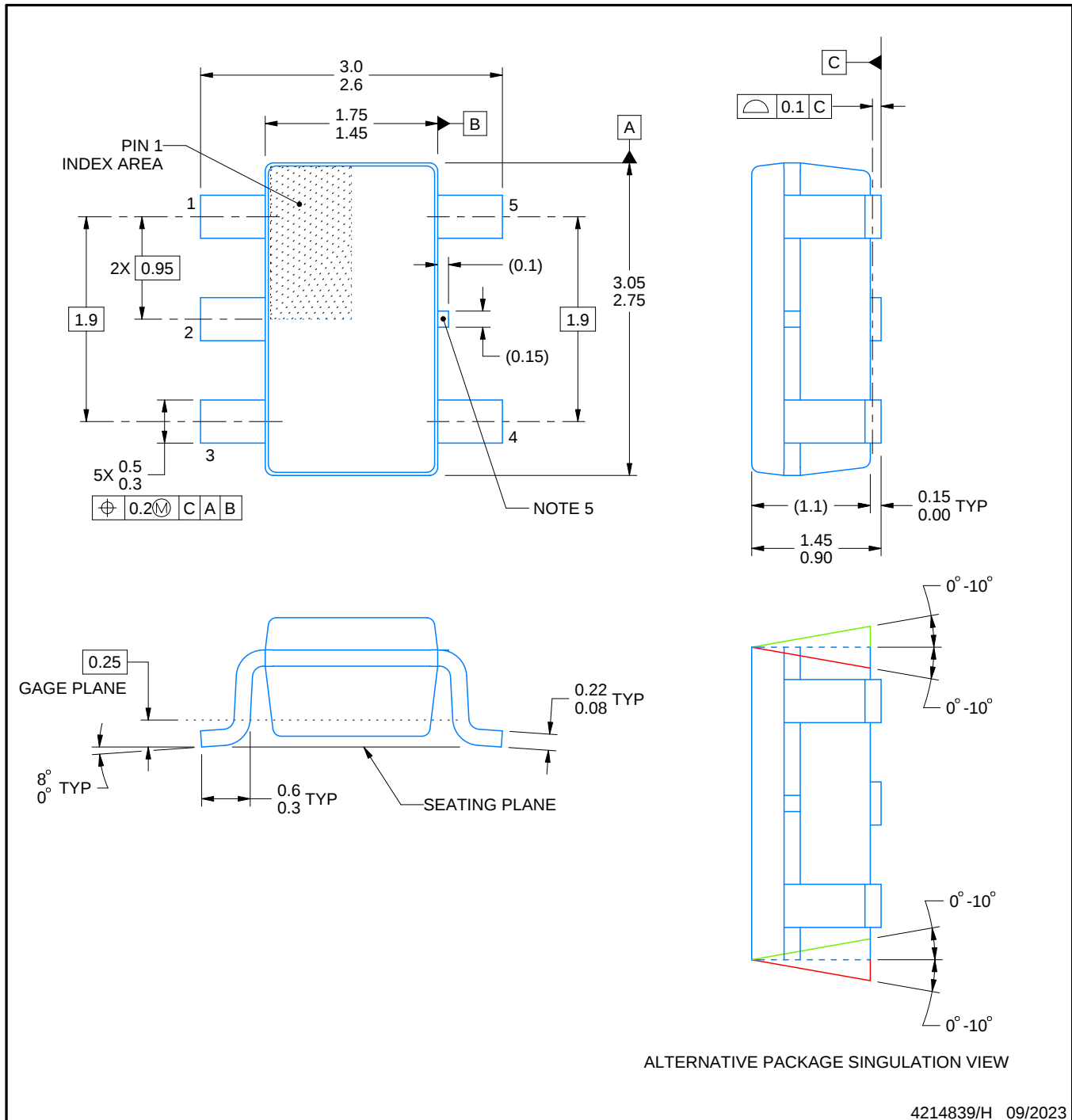


SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



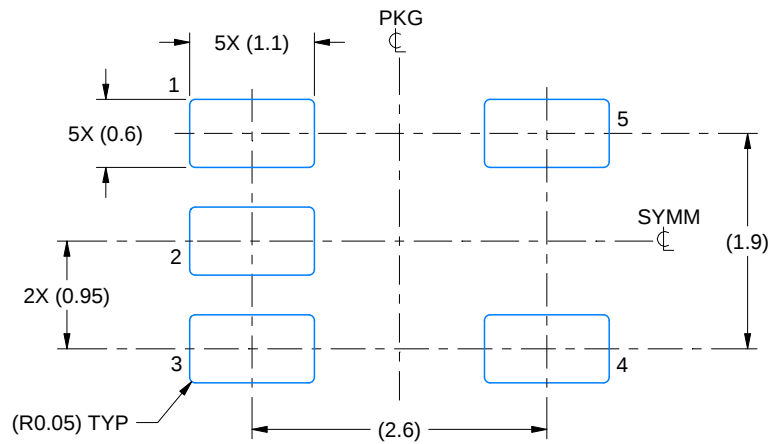
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

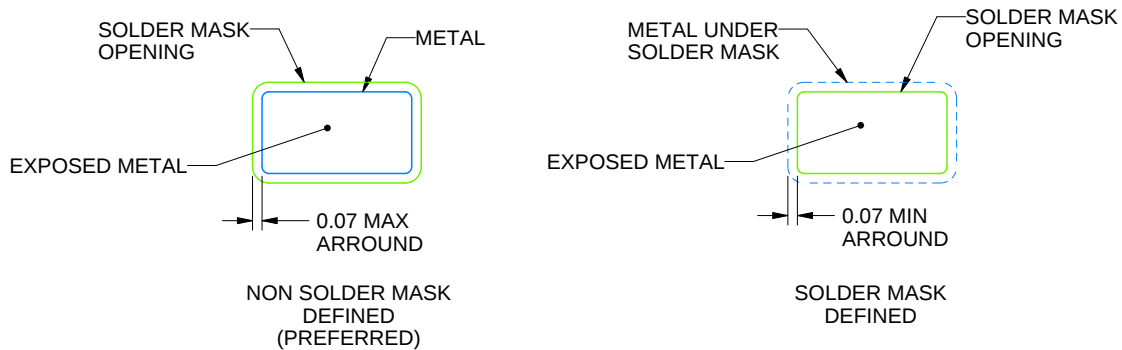
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/H 09/2023

NOTES: (continued)

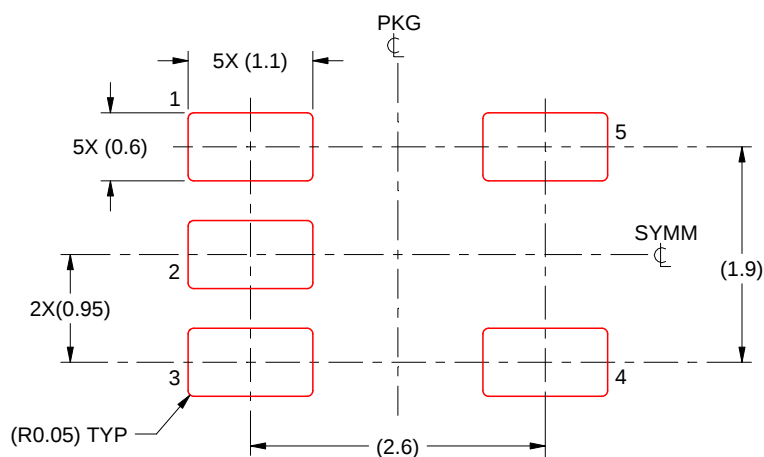
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

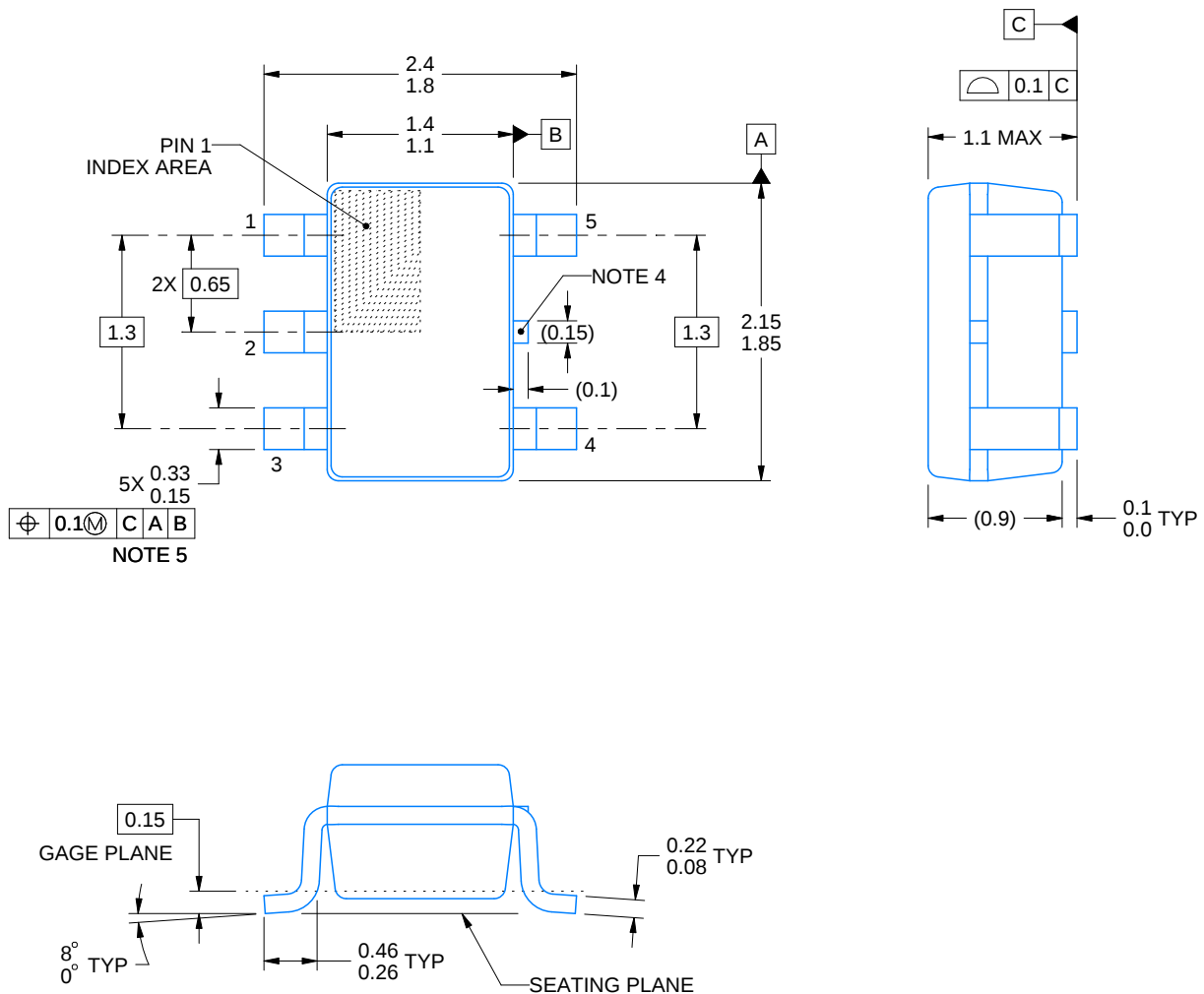


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/H 09/2023

NOTES: (continued)

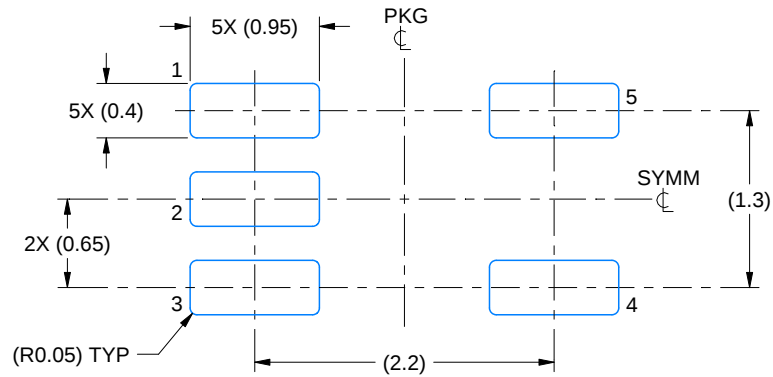
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



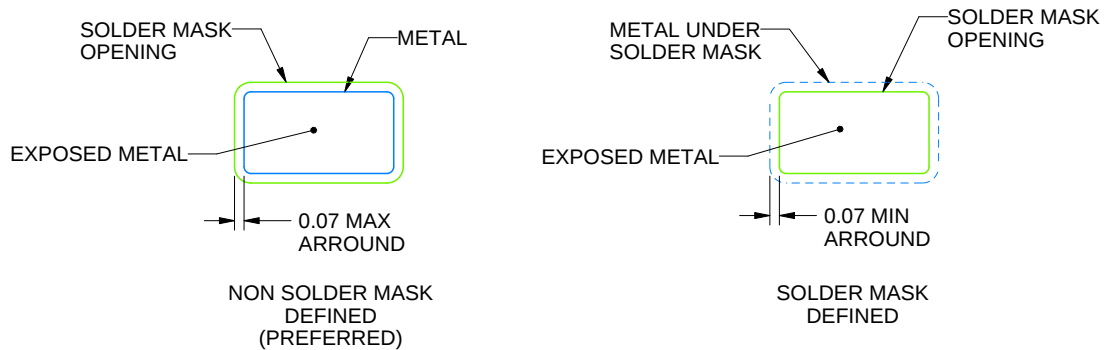
4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

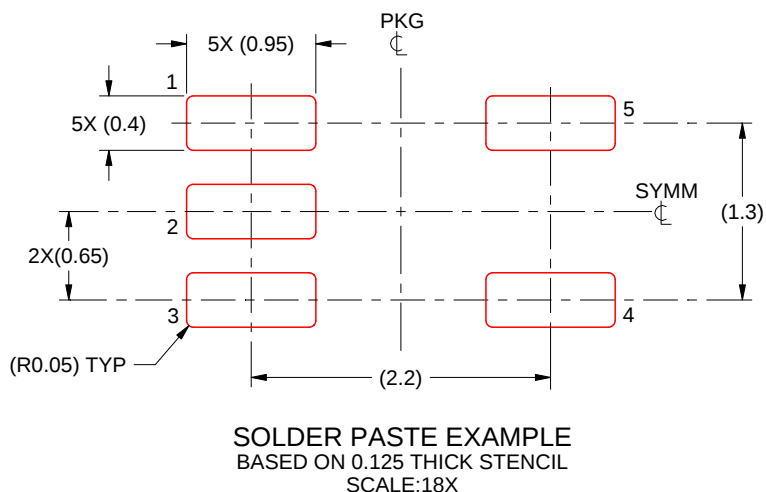


SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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